

CWDM7511P3N

SURFACE MOUNT SILICON
N-CHANNEL
ENHANCEMENT-MODE
MOSFET



SOIC-8 CASE

Central
Semiconductor

www.centrasemi.com

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CWDM7511P3N is a high current silicon N-Channel enhancement-mode MOSFET designed for high speed pulsed amplifier and driver applications. This energy efficient MOSFET offers beneficially low $r_{DS(ON)}$, and low threshold voltage.

MARKING CODE: 11P3N

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

Drain-Source Voltage

Gate-Source Voltage

Continuous Drain Current

Continuous Drain Current ($T_A=10^\circ\text{C}$, $T_J=25^\circ\text{C}$)

Operating and Storage Junction Temperature

Power Dissipation

SYMBOL

V_{DS}

75

UNITS

V

V_{GS}

20

V

I_D

8.3

A

I_D

11.3

A

T_J , T_{stg}

-55 to +150

$^\circ\text{C}$

P_D

2.5

W

ELECTRICAL CHARACTERISTICS: ($T_A=25^\circ\text{C}$ unless otherwise noted)

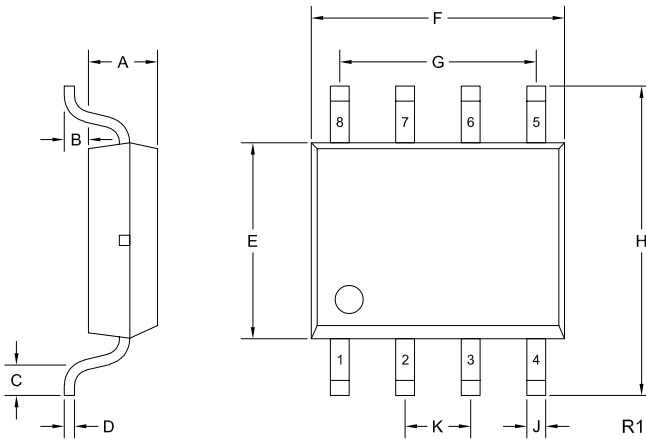
SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{GSSF} , I_{GSSR}	$V_{GS}=20\text{V}$, $V_{DS}=0$			100	nA
I_{DSS}	$V_{DS}=60\text{V}$, $V_{GS}=0$			1.0	μA
BV_{DSS}	$V_{GS}=0$, $I_D=250\mu\text{A}$	75			V
$V_{GS(th)}$	$V_{GS}=V_{DS}$, $I_D=250\mu\text{A}$	2.0	2.7	4.1	V
V_{SD}	$V_{GS}=0$, $I_S=1.0\text{A}$			1.6	V
$r_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=1.0\text{A}$		18	22	m Ω
C_{iss}	$V_{DS}=75\text{V}$, $V_{GS}=0$		3.0		nF
C_{oss}	$V_{DS}=75\text{V}$, $V_{GS}=0$		0.13		nF
C_{rss}	$V_{DS}=75\text{V}$, $V_{GS}=0$		0.04		nF
$t_{d(on)}$	$V_{DS}=75\text{V}$, $V_{GS}=10\text{V}$, $R_{DL}=75\Omega$		7.7		ns
t_r	$V_{DS}=75\text{V}$, $V_{GS}=10\text{V}$, $R_{DL}=75\Omega$		4.5		ns
$t_{d(off)}$	$V_{DS}=75\text{V}$, $V_{GS}=10\text{V}$, $R_{DL}=75\Omega$		31.5		ns
t_f	$V_{DS}=75\text{V}$, $V_{GS}=10\text{V}$, $R_{DL}=75\Omega$		47.3		ns

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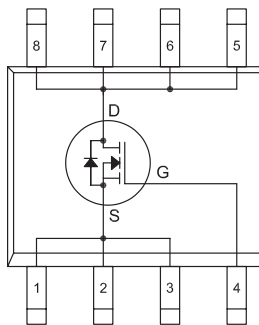
SOIC-8 CASE - MECHANICAL OUTLINE



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.061	1.392	1.554
B	0.004	0.009	0.100	0.224
C	0.016	0.035	0.40	0.90
D	0.007	0.010	0.19	0.25
E	0.145	0.157	3.80	4.00
F	0.189	0.198	4.80	5.00
G	0.150		3.81	
H	0.228	0.244	5.80	6.20
J	0.013	0.020	0.33	0.51
K	0.050		1.27	

SOIC-8 (REV: R1)

PIN CONFIGURATION

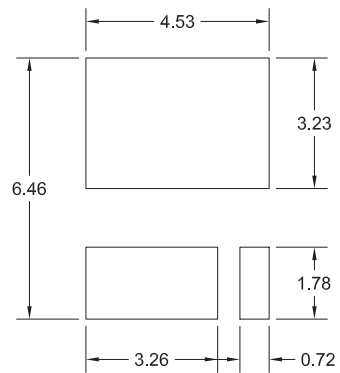


LEAD CODE:

- 1) Source 5) Drain
- 2) Source 6) Drain
- 3) Source 7) Drain
- 4) Gate 8) Drain

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SUGGESTED MOUNTING PADS
(Dimensions in mm)



R0

R2 (4-December 2023)

OUTSTANDING SUPPORT AND SUPERIOR SERVICES



PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

REQUESTING PRODUCT PLATING

1. If requesting Tin/Lead plated devices, add the suffix "TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
2. If requesting Lead (Pb) Free plated devices, add the suffix "PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

CONTACT US

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