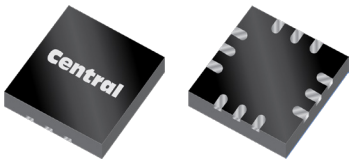
CQFGD1003

HALF-BRIDGE GaN
TRI-STATE PWM INPUTS
GATE DRIVER
100 VOLT



QFN3X3 CASE

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CQFGD1003 is a 100V half-bridge driver designed forefficient driving of gallium nitride (GaN) field-effect transistors (FETs), customized to address challenges commonly encountered in conventional MOSFET drivers.The CQFGD1003 optimizes gate switching timing by monitoring true gate voltages to achieve near zero dead time, enhancing efficiency and enabling high-frequency operation applications. The CQFGD1003 features a tri-state PWM input, allowing it to be driven high, low, or left floating for both sides of switches off. Its strong driving capability and fast propagation delay make it suitable for high-power and high frequency applications.

MARKING CODES

Line 1: Full Part Number

Line 2: Lot Code

Line 3: Date Code

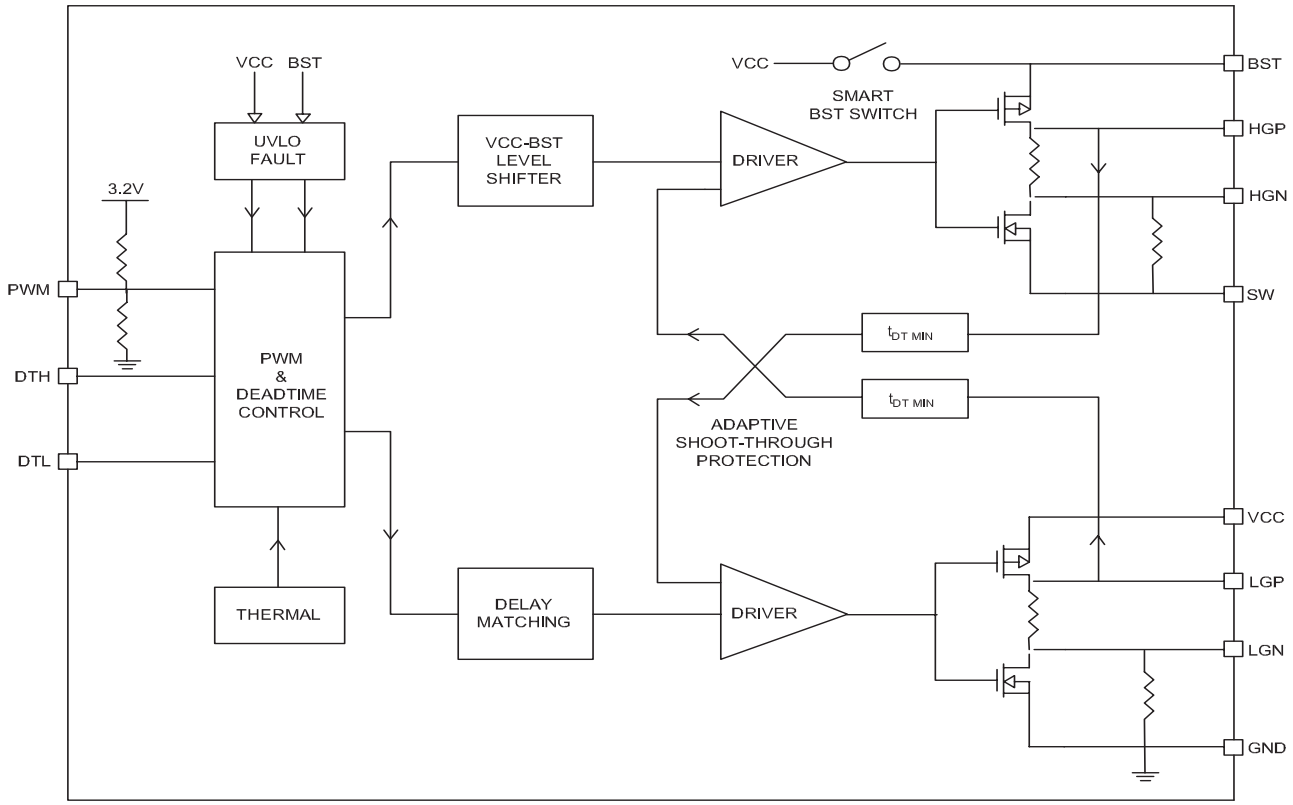
APPLICATIONS:

- Half-Bridge and Full-Bridge Converters
- High-Voltage DC-DC Converters
- 48V DC Motor Drive
- Automotive 48V/12V Bi-directional DC-DC
- High Power Class-D Audio Power Amplifier
- High Frequency, High Power Density Applications

FEATURES:

- Single Tri-State PWM Input
- Strong 1-Ω Pullup and 0.2-Ω Pulldown Resistance
- Split Outputs for Adjustable Turn-on/-off Speeds
- Fast Propagation Delay (22ns Typical)
- Adjustable Dead Time Optimized for GaN FETs
- Built-In UVLO, OVP, OTP Protections
- High-Side Floating Supply Operates up to 100V

BLOCK DIAGRAM



R2 (31-July 2026)

CQFGD1003

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TRI-STATE PWM INPUTS
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MAXIMUM RATINGS: (T_A=25°C unless otherwise noted)

	SYMBOL		UNITS
Supply Voltage	V_{CC}	-0.3 to 6.0	V
High-Side Gate Driver Bootstrap Supply to Switch Node	BST to SW	-0.3 to 6.0	V
PWM Input, Dead Time Setting for Low-to-High High-to-Low	PWM, DTH, DTL	-0.3 to 6.0	V
High-Side Gate Driver Pull-Up/ Pull-Down Output	HGP, HGN	SW-0.3 to BST+0.3	V
Low-Side Gate Driver Pull-Up/ Pull-Down Output	LGP, LGN	-0.3 to V_{CC}+0.3	V
Switch Node	SW	-5 to 100	V
High-Side Gate Driver Bootstrap Supply	BST	-0.3 to 105	V
Operating Junction Temperature	T_J	-40 to +150	°C
Storage Junction Temperature	T_{stg}	-55 to +150	°C
Human Body Model	HBM	±2000	V
Charged Device Model	CDM	±1000	V
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	68.82	°C/W
Junction to Case Top Thermal Resistance	$R_{\theta JC(TOP)}$	59.65	°C/W
Junction to Board Thermal Resistance	$R_{\theta JB}$	16.94	°C/W

ELECTRICAL CHARACTERISTICS: (T_J=25°C, V_{CC}=BST=5V, SW=GND=0V, HGP=HGN=HG, LGP=LGN=LG unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{CC\ Q}$	PWM=High-Z, R_{DTH}=R_{DTL}=75kΩ		360	600	µA
$I_{CC\ OP}$	f=500kHz		1.5	3.0	mA
$I_{BST\ Q}$	PWM=High-Z		40	70	µA
$I_{BST\ OP}$	f=500kHz		1.5	3.0	mA
$V_{CC\ OVR}$	*above*	5.7	6.0	6.3	V
$V_{CC\ OVHYS}$	*above*		0.25		V
$V_{CC\ UVR}$	*above*	3.9	4.1	4.3	V
$V_{CC\ UVHYS}$	*above*		0.3		V
$V_{BST\ UVR}$	*above*		3.6		V
$V_{BST\ UVHYS}$	*above*		0.5		V
V_{IH}	PWM rising	2.0	2.2	2.4	V
$V_{IH\ HYS}$	*above*	0.1	0.2	0.3	V
V_{IL}	PWM falling	0.8	1.0	1.2	V
$V_{IL\ HYS}$	*above*	0.1	0.2	0.3	V
V_{TRI}	*above*	1.4	1.6	1.8	V
R_{IUP}	To internal 3.2V supply		10		kΩ
R_{IDN}	*above*		10		kΩ
$V_{F\ low}$	$I_{VCC\ BST}$=100µA		0.02	0.2	V
$V_{F\ high}$	$I_{VCC\ BST}$=100mA		0.4		V
$R_{BST(ON)}$	*above*		4.0		Ω
R_{DN}	I_{HGN} or I_{LGN}=100mA		0.2	1.0	Ω
R_{UP}	I_{HGP} or I_{LGP}=-100mA		1.0	2.0	Ω
I_{OH}	HG=SW or LG=GND		1.7		A
I_{OL}	HG=BST or LG=VCC		4.3		A

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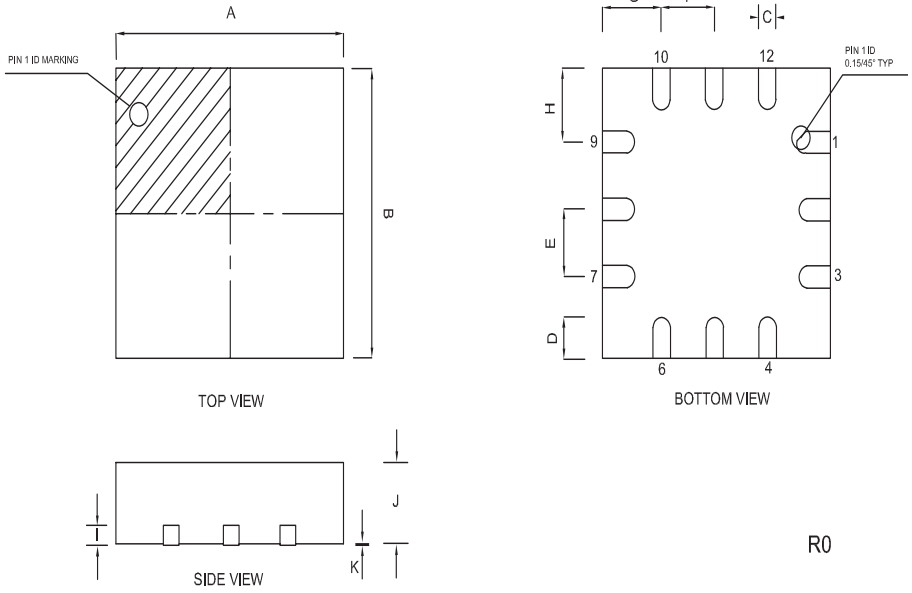
ELECTRICAL CHARACTERISTICS - Continued: (T_J=25°C, V_{CC}=BST=5V, SW=GND=0V, HGP=HGN=HG, LGP=LGN=LG unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{DT}	*above*		1.21		V
T_{OTP}	*above*		165		°C
$T_{OTP\ HYS}$	*above*		20		°C
T_{IPW}	*above*		5.0		ns
T_{OPW}	*above*		55		ns
T_R	C_L=1nF, 10% to 90%		7.0		ns
T_F	C_L=1nF, 90% to 10%		3.0		ns
T_{DTH}	R_{DTH}=36kΩ		2.0		ns
T_{DTH}	R_{DTH}=270kΩ		15		ns
T_{DTL}	R_{DTL}=36kΩ		2.0		ns
T_{DTL}	R_{DTL}=270kΩ		15		ns
T_{HPHL}	PWM falling to HG falling		22		ns
T_{LPHL}	PWM rising to LG falling		22		ns

QFN3X3 CASE - MECHANICAL OUTLINE



DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.114	0.122	2.90	3.10
B	0.114	0.122	2.90	3.10
C	0.008	0.011	0.20	0.30
D	0.018	0.026	0.45	0.65
E	0.026		0.65	
F	0.026		0.65	
G	0.033		0.85	
H	0.033		0.85	
I	0.008		0.20	
J	0.029	0.037	0.75	0.95
K	0.000	0.002	0.00	0.05

QFN3X3 (REV: R0)

R0

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LEAD CODE:

Pin Number	Pin Name	Description
1	LGP	Low-Side Gate Driver Pull-Up Output. Connect to the gate of the low-side GaN FET. Use a resistor to adjust the turn-on speed.
2,6	SW	Switch Node. Connect to the negative terminal of the bootstrap capacitor, the source of the high-side GaN FET, and the drain of the low-side GaN FET.
3	HGN	High-Side Gate Driver Pull-Down Output. Connect to the gate of the high-side GaN FET. Use a resistor to adjust the turn-off speed.
4	HGP	High-Side Gate Driver Pull-Up Output. Connect to the gate of the high-side GaN FET. Use a resistor to adjust the turn-on speed.
5	BST	High-Side Gate Driver Bootstrap Supply. Locally bypass this pin to SW with a ceramic bootstrap capacitor.
7	DTL	Dead Time Setting for High-to-Low Transition. Connect a resistor to GND.
8	PWM	PWM Input. This pin receives tri-state input and controls the driver outputs.
9	DTH	Dead Time Setting for Low-to-High Transition. Connect a resistor to GND.
10	VCC	IC and Low-Side Gate Driver Supply. Locally bypass this pin to GND with a ceramic capacitor.
11	GND	Ground. All signals are referenced to this ground.
12	LGN	Low-Side Gate Driver Pull-Down Output. Connect to the gate of the low-side GaN FET. Use a resistor to adjust the turn-off speed.

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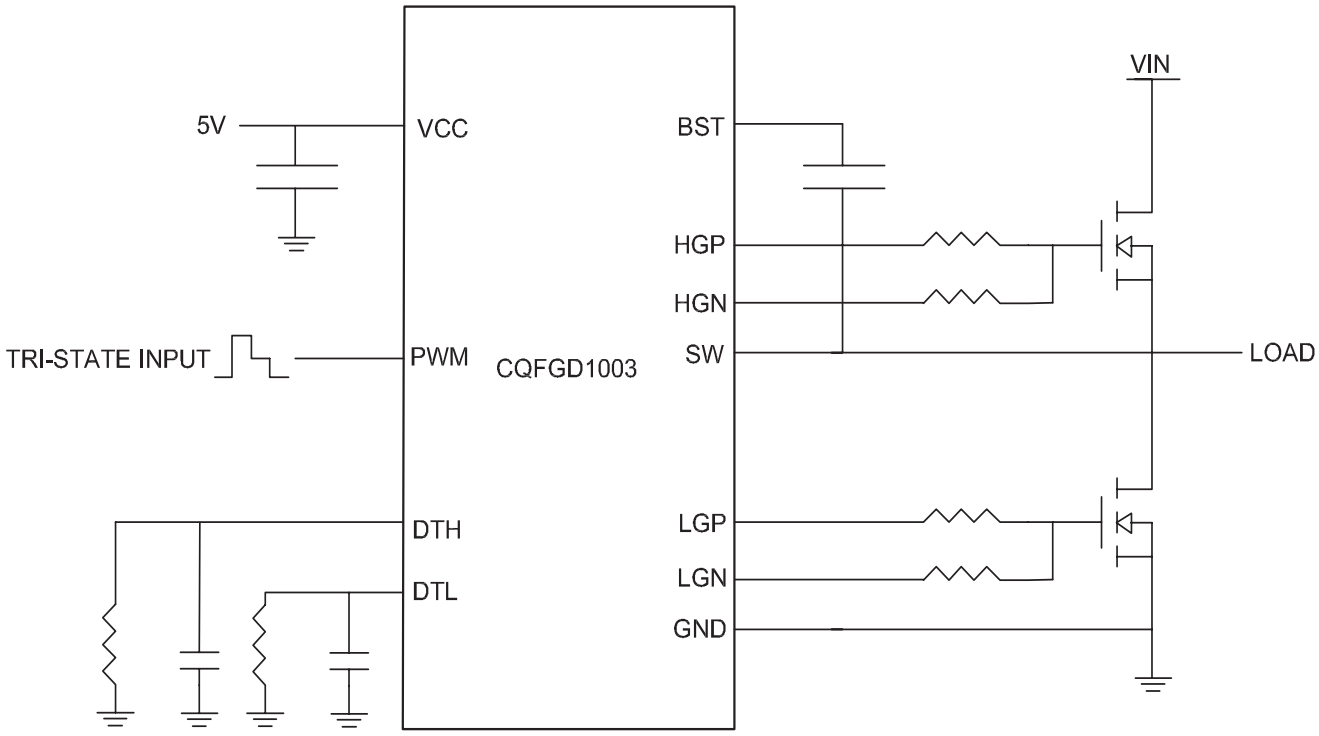
TYPICAL APPLICATION DRAWING



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RECOMMENDED COMPANION CENTRAL GAN FETS

Part Number	Rating	Package	Typical Applications
CCSPG1060N	100V, 60A	CSP3.5X5	Compact 48V DC-DC converters, telecom, point-of-load power
CCSPG1560N	150V, 60A	CSP4X6	48V DC-DC converters, motor drives, Class-D audio
CCSPG1510N	150V, 100A	CSP4X6	High-current 48V systems, bidirectional converters

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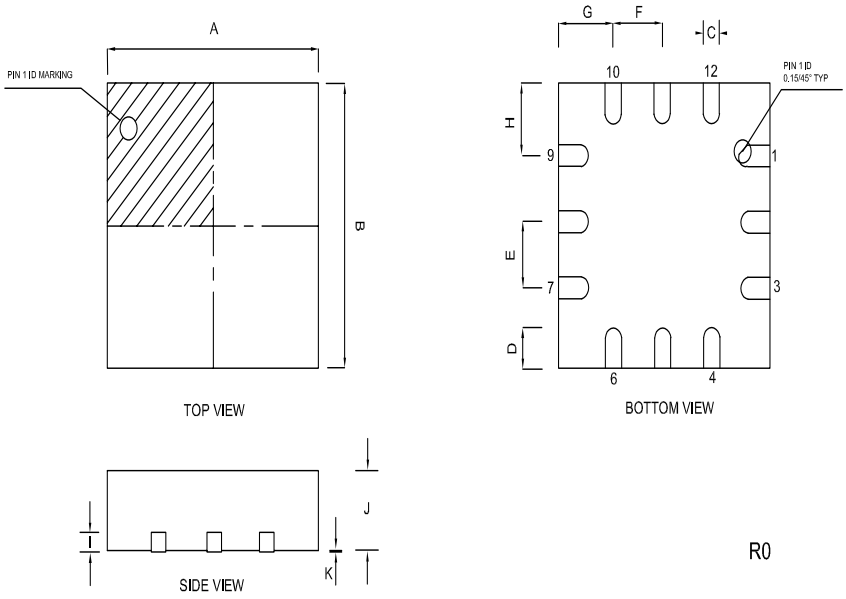
Package Details
QFN3X3 Case

Mechanical Drawing



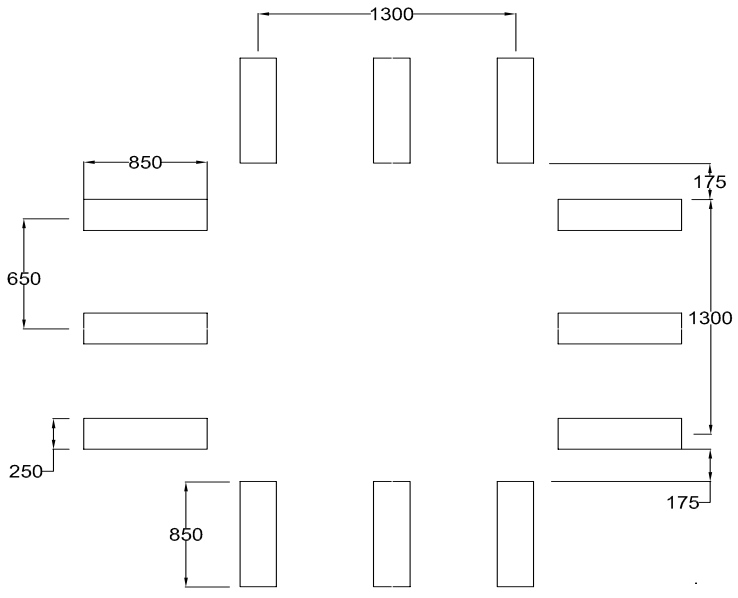
R0

DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.114	0.122	2.90	3.10
B	0.114	0.122	2.90	3.10
C	0.008	0.011	0.20	0.30
D	0.018	0.026	0.45	0.65
E	0.026		0.65	
F	0.026		0.65	
G	0.033		0.85	
H	0.033		0.85	
I	0.008		0.20	
J	0.029	0.037	0.75	0.95
K	0.000	0.002	0.00	0.05

QFN3X3 (REV: R0)

Part Marking: Line 1: Full Part Number, Line 2: Lot Code, Line 3: Date Code

Mounting Pad Geometry (Dimensions in mm)



TOP VIEW R0

R0 (17-February 2026)