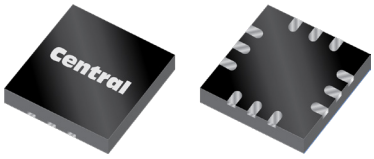
CQFGD1002

HALF-BRIDGE GaN
DUAL PWM INPUTS
GATE DRIVER
100 VOLT



QFN3X3 CASE

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CQFGD1002 is a 100V half-bridge driver designed to efficiently drive both high-side and low-side gallium nitride (GaN) field effect transistor (FET). Specifically designed for GaN FETs, the CQFGD1002 solves numerous challenges traditionally faced with conventional MOSFET driver solutions. The CQFGD1002 has two logic inputs to control high-side and low-side drivers independently for maximum flexibility, and drivers have split outputs to adjust turnon and turn-off speeds separately. The strong driving capability and excellent delay matching make the CQFGD1002 suitable for high power and high frequency aplications.

MARKING CODES

Line 1: Full Part Number

Line 2: Lot Code

Line 3: Date Code

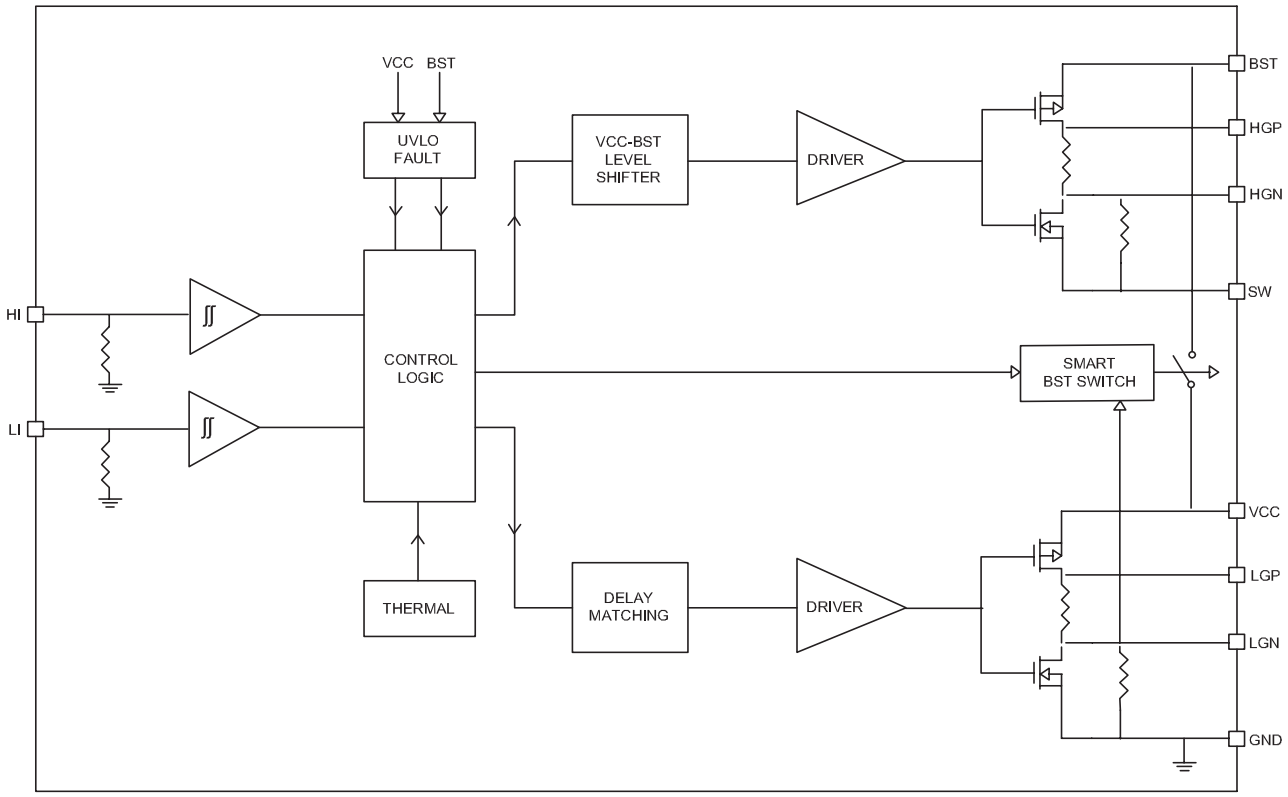
APPLICATIONS:

- Half-Bridge and Full-Bridge Converters
- High-Voltage DC-DC Converters
- 48V DC Motor Drive
- Automotive 48V/12V Bi-directional DC-DC
- High Power Class-D Audio Power Amplifier
- High Frequency, High Power Density Applications

FEATURES:

- Independent High-Side & Low-Side Logic Inputs
- Strong 1-Ω Pullup and 0.2-Ω Pulldown Resistance
- Split Outputs for Adjustable Turn-on/-off Speeds
- Fast Propagation Delay (14ns Typical)
- Excellent Delay Matching (1ns Typical)
- Built-In UVLO, OVP, OTP Protections
- High-Side Floating Supply Operates up to 100V

BLOCK DIAGRAM



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MAXIMUM RATINGS: (T_A=25°C unless otherwise noted)

	SYMBOL		UNITS
Supply Voltage	V_{CC}	-0.3 to 6.0	V
High-Side Gate Driver Bootstrap Supply to Switch Node	BST to SW	-0.3 to 6.0	V
High-Side/ Low-Side Gate Driver Control Input, No Function Connection	HI, LI, NC	-0.3 to 6.0	V
High-Side Gate Driver Pull-Up/ Pull-Down Output	HGP, HGN	SW-0.3 to BST+0.3	V
Low-Side Gate Driver Pull-Up/ Pull-Down Output	LGP, LGN	-0.3 to V_{CC}+0.3	V
Switch Node	SW	-5 to 100	V
High-Side Gate Driver Bootstrap Supply	BST	-0.3 to 105	V
Operating Junction Temperature	T_J	-40 to +150	°C
Storage Junction Temperature	T_{stg}	-55 to +150	°C
Human Body Model	HBM	±2000	V
Charged Device Model	CDM	±1000	V
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	68.82	°C/W
Junction to Case Top Thermal Resistance	$R_{\theta JC(TOP)}$	59.65	°C/W
Junction to Board Thermal Resistance	$R_{\theta JB}$	16.94	°C/W

ELECTRICAL CHARACTERISTICS: (T_J=25°C, V_{CC}=BST=5V, SW=GND=0V, HGP=HGN, LGP=LGN unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{CC\ Q}$	HI=LI=0V		35	60	µA
$I_{CC\ OP}$	f=500kHz		1.0	2.0	mA
$I_{BST\ Q}$	HI=LI=0V		40	70	µA
$I_{BST\ OP}$	f=500kHz		1.0	2.0	mA
$V_{CC\ OVR}$	*above*	5.7	6.0	6.3	V
$V_{CC\ OVHYS}$	*above*		0.25		V
$V_{CC\ UVR}$	*above*	3.9	4.1	4.3	V
$V_{CC\ UVHYS}$	*above*		0.3		V
$V_{BST\ UVR}$	*above*		3.6		V
$V_{BST\ UVHYS}$	*above*		0.5		V
V_{IH}	*above*		1.8	2.2	V
V_{IL}	*above*	0.8	1.2		V
$V_{I\ HYS}$	*above*		0.6		V
R_I	*above*		200		kΩ
$V_{F\ low}$	$I_{VCC\ BST}$=100µA		0.02	0.2	V
$V_{F\ high}$	$I_{VCC\ BST}$=100mA		0.4		V
$R_{BST(ON)}$	*above*		4.0		Ω
R_{DN}	I_{HGN} or I_{LGN}=100mA		0.2	1.0	Ω
R_{UP}	I_{HGP} or I_{LGP}=-100mA		1.0	2.0	Ω
I_{OH}	HG=SW or LG=GND		1.7		A
I_{OL}	HG=BST or LG=VCC		4.3		A
T_{OTP}	*above*		165		°C
$T_{OTP\ HYS}$	*above*		20		°C

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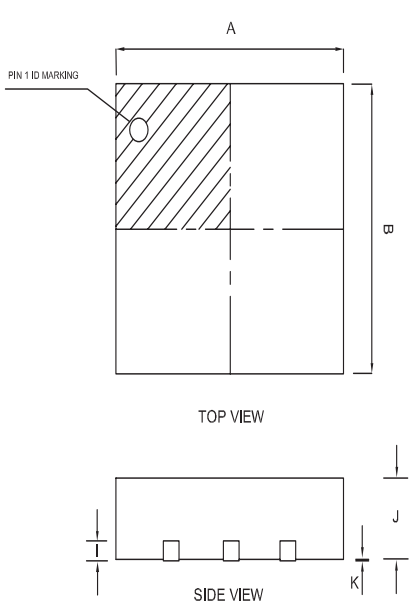
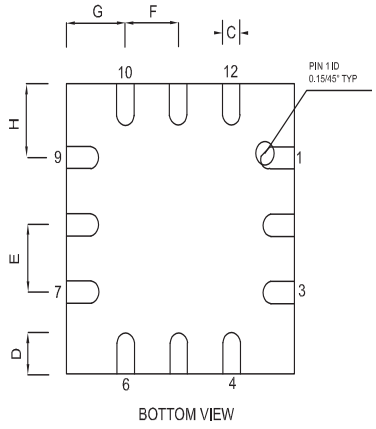
ELECTRICAL CHARACTERISTICS - Continued: (T_J=25°C, V_{CC}=BST=5V, SW=GND=0V, HGP=HGN, LGP=LGN unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
T_{IPW}	*above*		5.0		ns
T_{OPW}	*above*		12		ns
T_R	C_L=1nF, 10% to 90%		7.0		ns
T_F	C_L=1nF, 90% to 10%		3.0		ns
T_{HPHL}	HI falling to HG falling		14		ns
T_{HPLH}	HI rising to HG rising		14		ns
T_{LPHL}	LI falling to LG falling		14		ns
T_{LPLH}	LI rising to LG rising		14		ns
T_{MON}	*above*		1.0	5.0	ns
T_{MOFF}	*above*		1.0	5.0	ns

QFN3X3 CASE - MECHANICAL OUTLINE





R0

DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.114	0.122	2.90	3.10
B	0.114	0.122	2.90	3.10
C	0.008	0.011	0.20	0.30
D	0.018	0.026	0.45	0.65
E	0.026		0.65	
F	0.026		0.65	
G	0.033		0.85	
H	0.033		0.85	
I	0.008		0.20	
J	0.029	0.037	0.75	0.95
K	0.000	0.002	0.00	0.05

QFN3X3 (REV: R0)

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LEAD CODE:

Pin Number	Pin Name	Description
1	LGP	Low-Side Gate Driver Pull-Up Output. Connect to the gate of the low-side GaN FET. Use a resistor to adjust the turn-on speed.
2,6	SW	Switch Node. Connect to the negative terminal of the bootstrap capacitor, the source of the high-side GaN FET, and the drain of the low-side GaN FET.
3	HGN	High-Side Gate Driver Pull-Down Output. Connect to the gate of the high-side GaN FET. Use a resistor to adjust the turn-off speed.
4	HGP	High-Side Gate Driver Pull-Up Output. Connect to the gate of the high-side GaN FET. Use a resistor to adjust the turn-on speed.
5	BST	High-Side Gate Driver Bootstrap Supply. Locally bypass this pin to SW with a ceramic bootstrap capacitor.
7	NC	No Function Connection. This pin can be left open, connected to VCC or GND.
8	HI	High-Side Gate Driver Control Input. This pin has an internal 200kΩ pull-down resistor.
9	LI	Low-Side Gate Driver Control Input. This pin has an internal 200kΩ pull-down resistor.
10	VCC	IC and Low-Side Gate Driver Supply. Locally bypass this pin to GND with a ceramic capacitor.
11	GND	Ground. All signals are referenced to this ground.
12	LGN	Low-Side Gate Driver Pull-Down Output. Connect to the gate of the low-side GaN FET. Use a resistor to adjust the turn-off speed.

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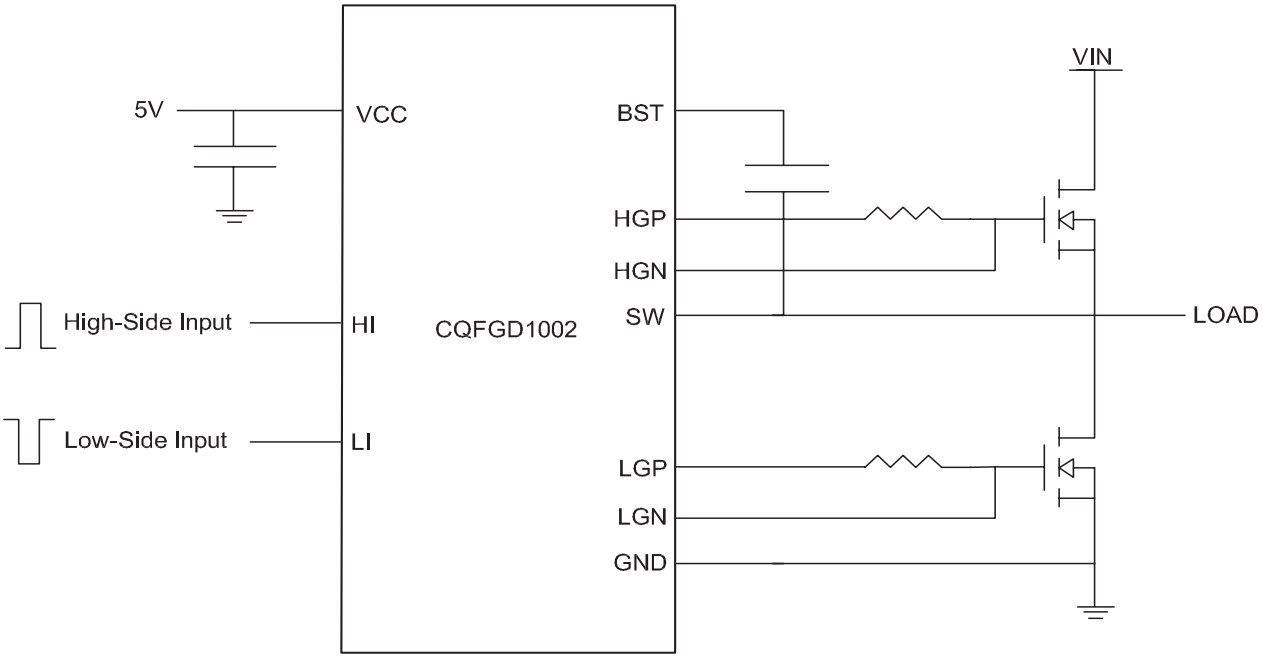
TYPICAL APPLICATION DRAWING



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RECOMMENDED COMPANION CENTRAL GAN FETS

Part Number	Rating	Package	Typical Applications
CCSPG1060N	100V, 60A	CSP3.5X5	Compact 48V DC-DC converters, telecom, point-of-load power
CCSPG1560N	150V, 60A	CSP4X6	48V DC-DC converters, motor drives, Class-D audio
CCSPG1510N	150V, 100A	CSP4X6	High-current 48V systems, bidirectional converters

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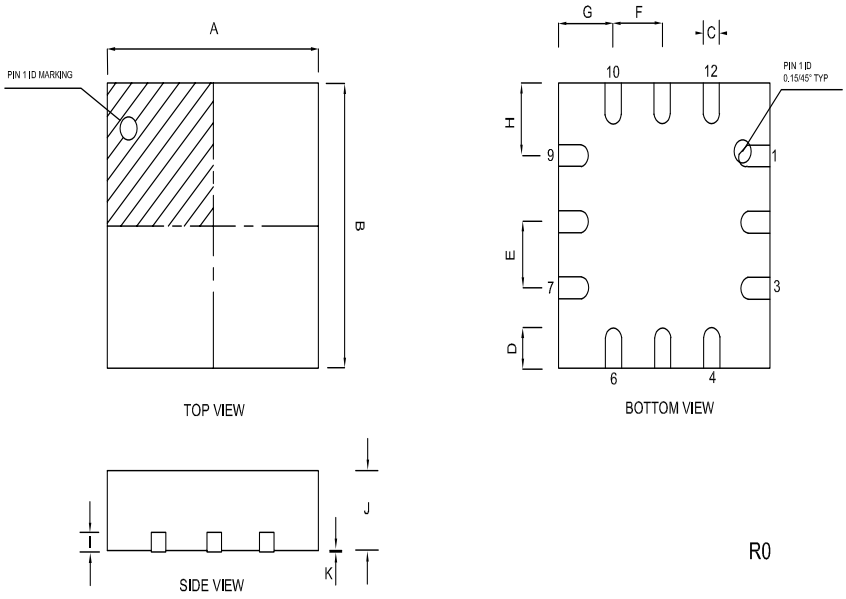
Package Details
QFN3X3 Case

Mechanical Drawing



R0

DIMENSIONS				
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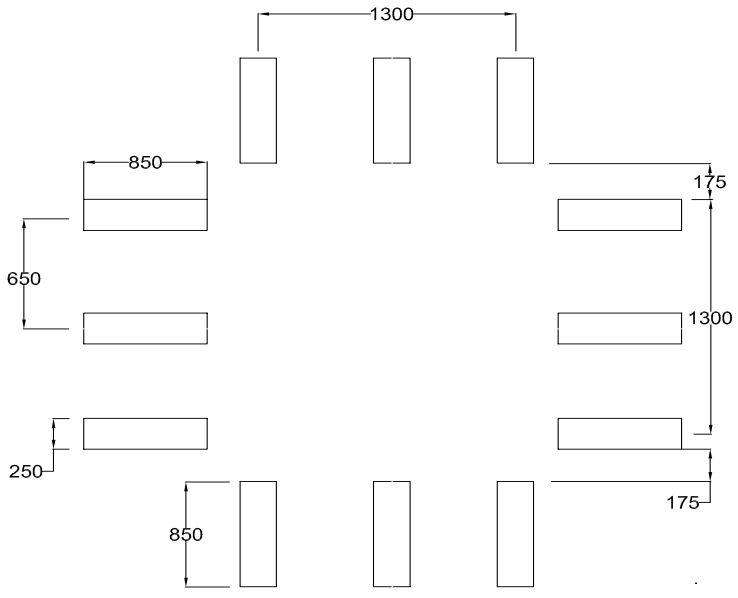
E	0.026		0.65	
F	0.026		0.65	
G	0.033		0.85	
H	0.033		0.85	
I	0.008		0.20	
J	0.029	0.037	0.75	0.95
K	0.000	0.002	0.00	0.05

QFN3X3 (REV: R0)

Part Marking: Line 1: Full Part Number, Line 2: Lot Code, Line 3: Date Code

Mounting Pad Geometry (Dimensions in mm)



TOP VIEW R0

R0 (17-February 2026)