CMPLD17-08 THRU CMPLD17-33

SURFACE MOUNT SILICON LOW DROPOUT REGULATOR 0.8 THRU 3.3 VOLT

SOT-25 CASE

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CDFLD SERIES is a high-performance, low-dropout linear regulator with 1.6V–6.5V input and 0.8V–3.3V output. With ultra-low quiescent current and built-in failsafe protection, it's ideal for compact, power-sensitive applications in portable electronics, sensors, and embedded systems.

MARKING CODES

CMPLD17-08: APAG01
CMPLD17-18: AVAE01
CMPLD17-28: AYAE01
CMPLD17-33: B1AE01

APPLICATIONS:

- Portable devices
- Consumer electronics
- Bluetooth headsets
- Fitness trackers
- Non-implant medical devices
- Smartphones and tablets
- RF and wireless communication

FEATURES:

- Input voltage range: 1.6V to 5.5V
- Output voltage range: 0.8V to 3.3V
- **Lo**w dropout voltage: 170mV at 300mA
- Ultra-low quiescent current: 25µA TYP
- Compatible with 1µF ceramic capacitors
- Built-in thermal and short-circuit protection

MAXIMUM RATINGS: (T_A=25°C unless otherwise noted)

	SYMBOL		UNITS
Voltage range at Input	V_{IN}	-0.3 to 6.5	V
Voltage range at Output	V_{OUT}	-0.3 to V_{IN}	V
Output Current	I_{OUT}	300	mA
Operating Junction Temperature	T_J	-40 to +150	°C
Storage Junction Temperature	T_{stg}	-65 to +150	°C
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	250	°C/W

ELECTRICAL CHARACTERISTICS: (T_J=25°C, V_{IN} = V_{OUT} + 1.0V, I_{OUT} = 1.0mA, C_{in} = C_{out} = 1.0µF unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	*above*	1.6		5.5	V
V_{OUT}	*above*	0.8		3.3	V
V_{OUT} Accuracy	$V_{OUT} \geq$ 2.0V	-0.1		1.0	%
I_{LIM}	V_{OUT}=0.9* V_{OUT} NOM		480		mA
V_{DO}	V_{OUT}=0.9*0.8V, I_{OUT}=300mA		950		mV
V_{DO}	V_{OUT}=0.9*1.8V, I_{OUT}=300mA		280		mV
V_{DO}	V_{OUT}=0.9*2.8V, I_{OUT}=300mA		170		mV
V_{DO}	V_{OUT}=0.9*3.3V, I_{OUT}=300mA		150		mV
ΔV_{OUT}/ (ΔV_{IN}*ΔV_{OUT})	V_{OUT} +1.0≤ V_{IN}≤5.5V		0.02		%/V
ΔV_{OUT}	I_{OUT}=0mA to 350mA			40	mV
I_Q	*above*		25		µA
I_{SC}	V_{OUT}=0		220		mA
I_{SHDN}	V_{EN}=0, V_{IN}=5.5V		0.1		µA

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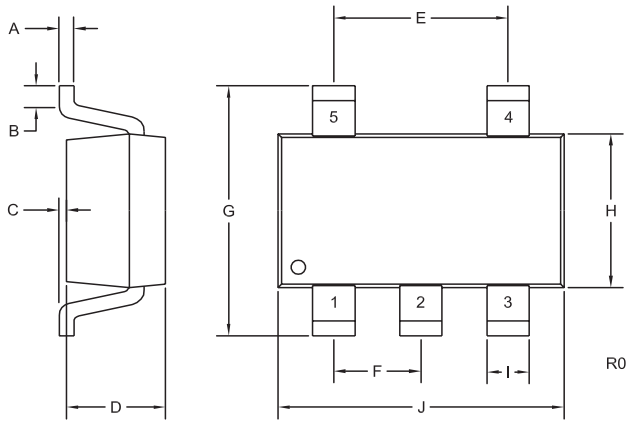
ELECTRICAL CHARACTERISTICS - Continued: (T_J=25°C, V_{IN} = V_{OUT} + 1.0V, I_{OUT} = 1.0mA, C_{in} = C_{out} = 1.0µF unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PSRR	I_{OUT}=20mA , f=100Hz		80		dB
PSRR	I_{OUT}=20mA , f=1kHz		75		dB
PSRR	I_{OUT}=20mA , f=10kHz		70		dB
PSRR	I_{OUT}=20mA , f=100kHz		60		dB
PSRR	I_{OUT}=20mA , f=1MHz		45		dB
V_{IH}	T_J=25°C	1.0			V
V_{IL}	T_J=25°C			0.4	V
I_{EN}	V_{EN}=5.5V		0.1		µA
e_n	f=10 to 100kHz, V_{OUT}=1.8V, I_{OUT}=1.0mA		50		µV/√Hz
T_{SDH}	I_{OUT}=1.0mA		175		°C
T_{SDL}	I_{OUT}=1.0mA		145		°C
R_{DISCH}	V_{EN}≤ 0.2V, V_{IN}=5.0V		100		Ω
t_{ON}	V_{EN}=HIGH, V_{OUT}=0.9* $V_{OUT\ NOM}$		120		µs

SOT-25 CASE - MECHANICAL OUTLINE



DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.004	0.007	0.11	0.19
B	0.016	-	0.40	-
C	-	0.004	-	0.10
D	0.039	0.047	1.00	1.20
E	0.074	0.075	1.88	1.92
F	0.037	0.038	0.93	0.97
G	0.102	0.118	2.60	3.00
H	0.059	0.067	1.50	1.70
I	0.016		0.41	
J	0.110	0.118	2.80	3.00

SOT-25 (REV: R0)

LEAD CODE:

1) VIN
2) GND
3) EN
4) NC
5) Vout

MARKING:

CMPLD17-08: APAG01
CMPLD17-18: AVAE01
CMPLD17-28: AYAE01
CMPLD17-33: B1AE01

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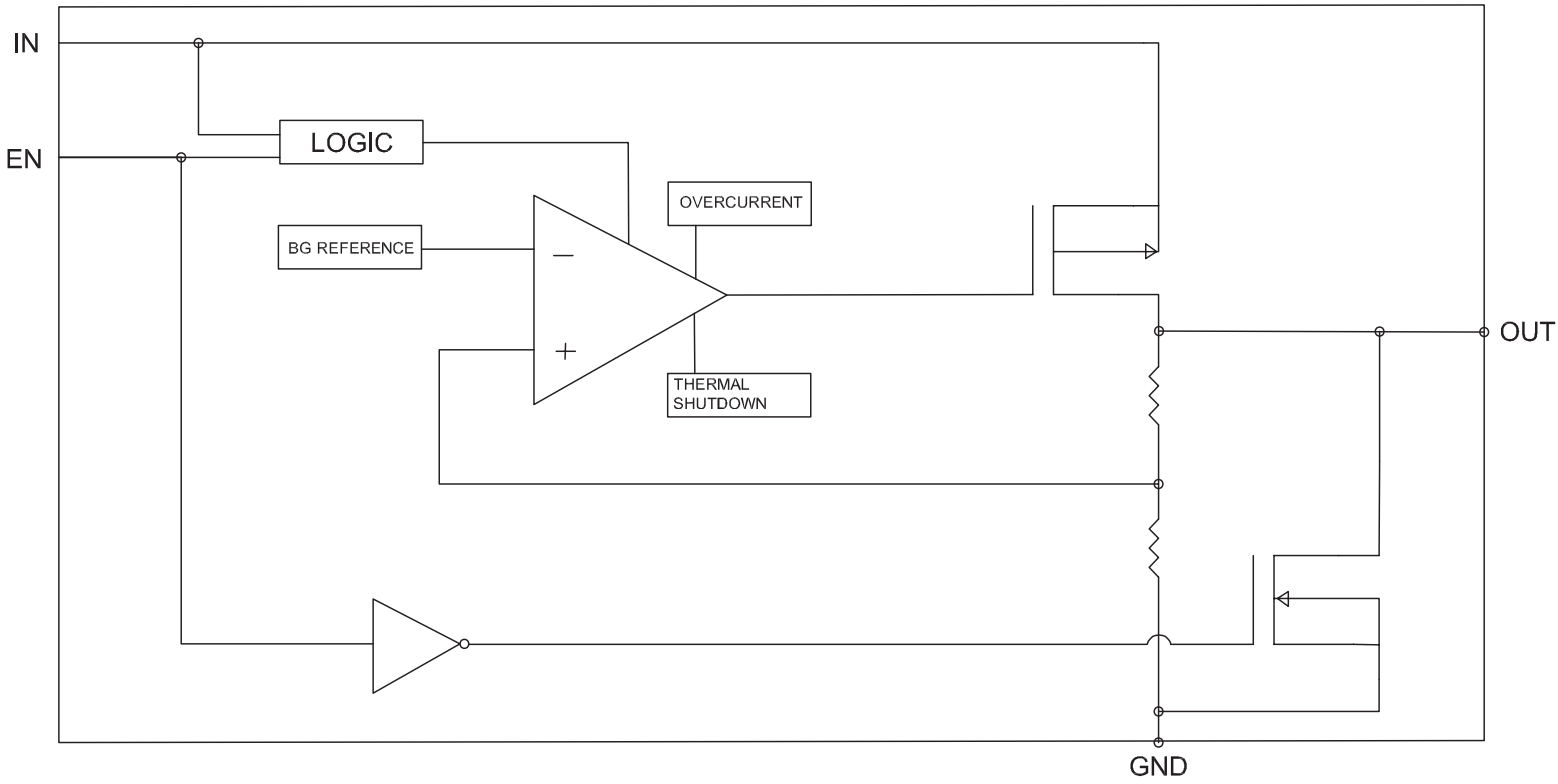
BLOCK DIAGRAM



LEAD CODE:

1) Input
2) Ground
3) Enable
4) NC
5) Vout

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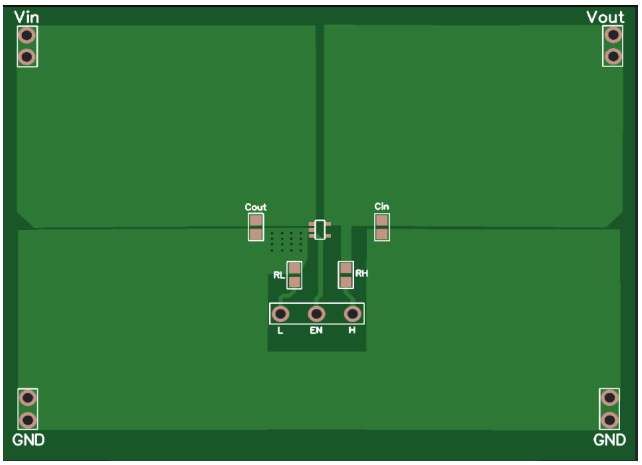
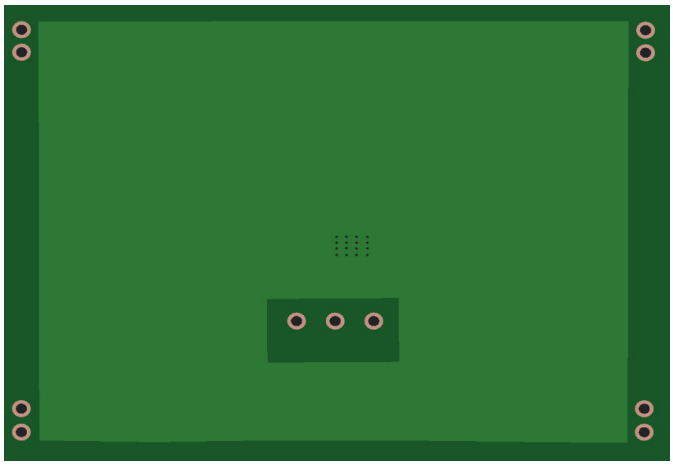
PCB DESIGN CONSIDERATIONS





- PCB dimensions: 98mm x 84mm
- Copper pad dimensions: 4x, 45mm x 32mm
- Outer copper weight: 2 oz
- Inner copper weight: 1 oz
- Place input and output capacitors as close to the device as possible
- Use copper planes for device connections and 4 PCB layers to optimize thermal performance
- Place thermal vias around the device to distribute the heat.

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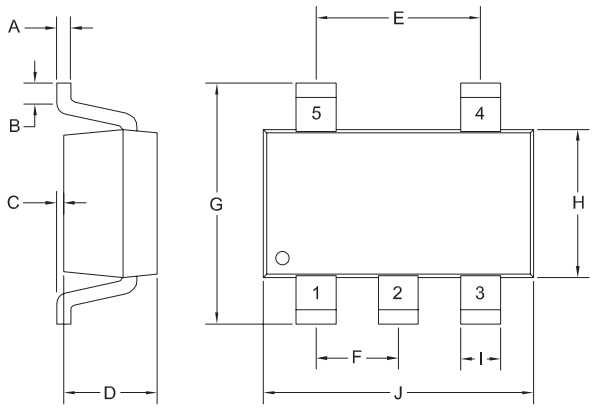
Package Details

SOT-25 Case

Mechanical Drawing



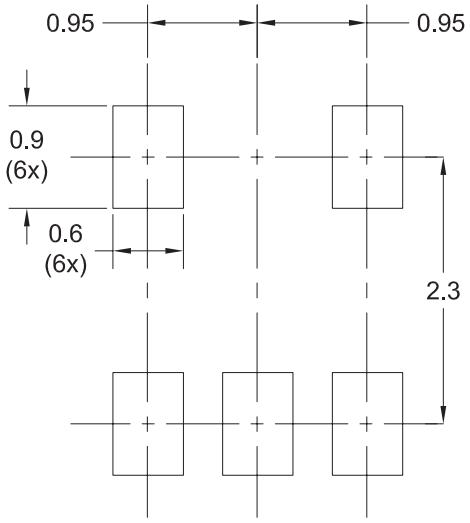
DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.004	0.008	0.11	0.20
B	0.012	0.024	0.30	0.60
C	-	0.006	-	0.15
D	0.039	0.047	1.00	1.20
E	0.071	0.079	1.80	2.00
F	0.035	0.039	0.90	1.00
G	0.102	0.118	2.60	3.00
H	0.059	0.067	1.50	1.70
I	0.014	0.018	0.36	0.45
J	0.110	0.118	2.80	3.00

SOT-25 (REV: R0)

R0

Part Marking: 6 Character Alpha/Numeric Code

Mounting Pad Geometry (Dimensions in mm)



R0 (26-February 2026)

OUTSTANDING SUPPORT AND SUPERIOR SERVICES

PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

REQUESTING PRODUCT PLATING

1. If requesting Tin/Lead plated devices, add the suffix " TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
2. If requesting Lead (Pb) Free plated devices, add the suffix " PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

CONTACT US

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