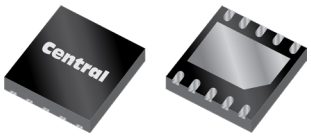
CDFGD1001

SINGLE-CHANNEL GaN GATE DRIVER 6.0 THRU 20 VOLT



DFN3X3 CASE

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CDFGD1001 is designed to drive single-channel GaN FET(s) in either low-side, high-side, or secondary-side SR applications. It has both non-inverting and inverting PWM inputs, working with controller, opto-coupler, and digital isolator flexibly. The strong driving capability and fast propagation delay, along with input noise deglitching and built-in UVLO, OVP, OTP protection features, make the CDFGD1001 extremely suitable for high power, high frequency, and robust power GaN applications. The CDFGD1001 is available in thermally enhanced DFN3x3 package.

MARKING CODES

Line 1: Full Part Number

Line 2: Lot Code

Line 3: Date Code

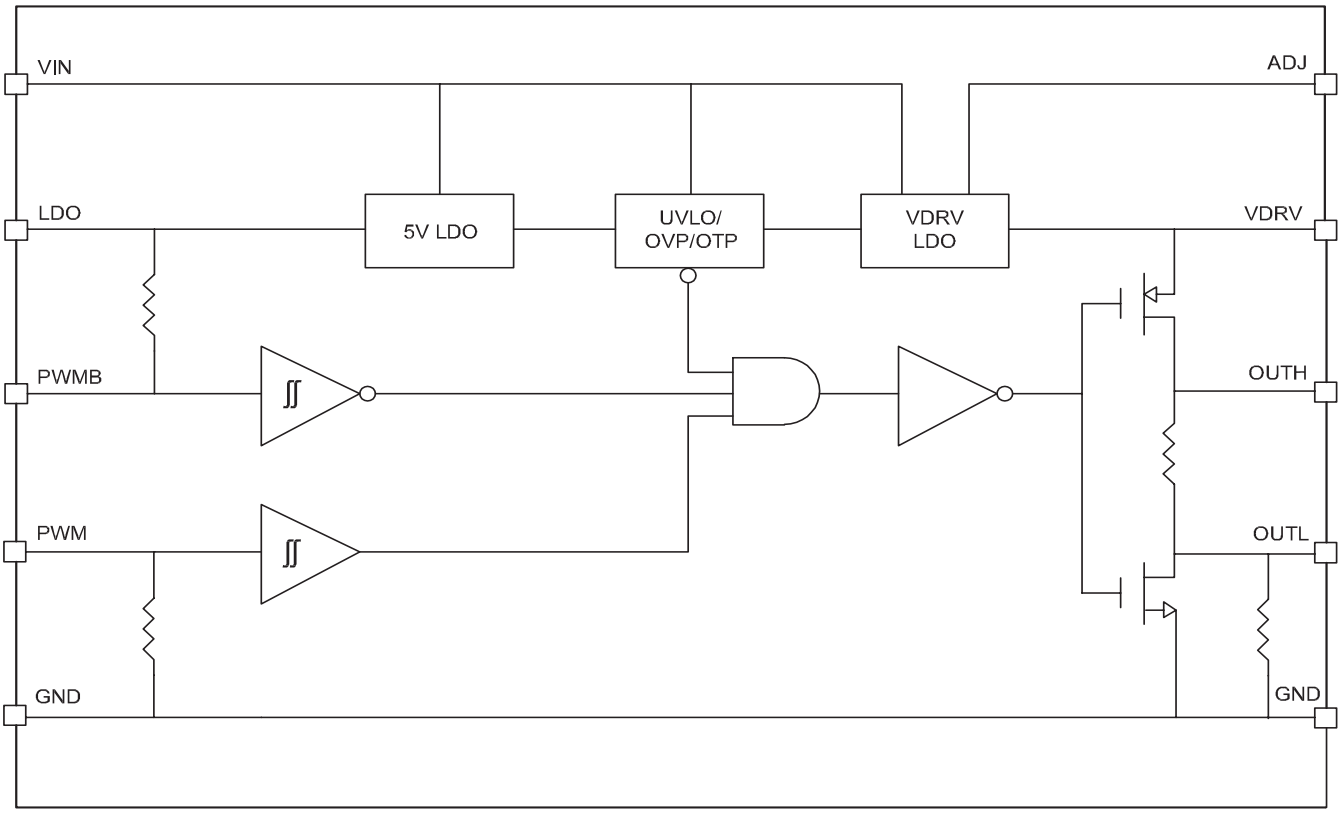
APPLICATIONS:

- Switch-Mode Power Supplies
- AC-AC, DC-DC Converters
- Solar Converters
- UPS
- Half-Bridge and Full-Bridge Converters
- Boost, Flyback, and Forward Converters

FEATURES:

- Wide 6V to 20V Operating Voltage Range
- Strong 1.3-Ω Pullup and 0.5-Ω Pulldown Resistance
- Fast Propagation Delay with Input Deglitching
- User Programmable Gate Driver Supply Voltage
- Integrated 5V LDO for supplying Digital Isolator
- Built-In UVLO, OVP, OTP Protection

BLOCK DIAGRAM



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MAXIMUM RATINGS: (T_A=25°C unless otherwise noted)

	SYMBOL		UNITS
Supply Input Voltage	V_{IN}	-0.3 to 22	V
Driver Voltage Output	V_{DRV}	-0.3 to 13.2	V
Pullup/Pulldown Voltage	OUTH, OUTL	-0.3 to V_{DRV} +0.3	V
PWM Inout, Inverting Input	PWM, PWMB	-0.3 to 6.0	V
5V LDO Output, Driver Voltage Adjustment	LDO, ADJ	-0.3 to 6.0	V
Operating Junction Temperature	T_J	-40 to +150	°C
Storage Junction Temperature	T_{stg}	-55 to +150	°C
Human Body Model	HBM	±2000	V
Charged Device Model	CDM	±1000	V
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	70.8	°C/W
Junction to Case Top Thermal Resistance	$R_{\theta JC(TOP)}$	67.2	°C/W
Junction to Case Bottom Thermal Resistance	$R_{\theta JC(BOT)}$	10.3	°C/W

ELECTRICAL CHARACTERISTICS: (T_A=25°C, V_{IN}=12V, C_{DRV}=1.0µF, C_{LDO}=1.0µF, OUTH=OUTL unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN\ UVLO}$	VIN rising		5.5	5.8	V
$V_{IN\ HYS}$	*above*		0.35		V
$I_{VIN\ Q}$	PMW=PWMB=0V		200		µA
V_{IH}	*above*		2.6	3.2	V
V_{IL}	*above*	0.8	1.4		V
R_{PWM}	To GND pin		200		kΩ
R_{PWMB}	To LDO pin		200		kΩ
V_{ADJ}	*above*	0.97	1	1.03	V
$V_{ADJ\ UVLO}$	ADJ rising	0.8	0.85	0.9	V
$V_{ADJ\ HYS}$	*above*		0.05		V
I_{DRV}	*above*	35	55	70	mA
$V_{DRV\ DO}$	V_{IN}=6V, ADJ=0V, I_{DRV}=20mA		140	250	mV
$V_{DRV\ OVP}$	V_{DRV} rising	11	11.5	12	V
$V_{DRV\ OVPHYS}$	*above*		0.5		V
V_{LDO}	*above*	4.85	5	5.15	V
$V_{LDO\ UVLO}$	LDO rising	3.8	4	4.2	V
$V_{LDO\ HYS}$	*above*		0.3		V
I_{LDO}	*above*		38		mA
$V_{LDO\ DO}$	V_{IN}=5V, I_{LDO}=10mA		130	250	mV
R_{OUTH}	V_{DRV}=6V, I_{OUTH}=-100mA		1.3		Ω
R_{OUTL}	I_{OUTL}=100mA		0.5		Ω
I_{OUTH}	*above*		2		A
I_{OUTL}	*above*		5.5		A
T_{SD}	*above*		160		°C
T_{HYS}	*above*		20		°C

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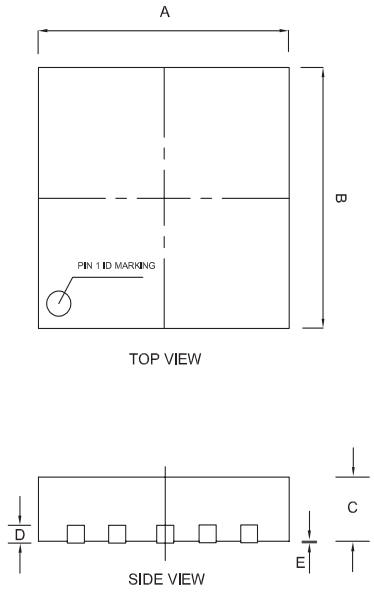
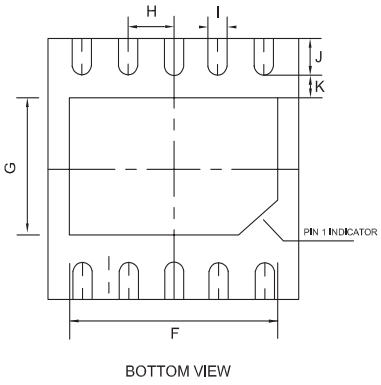
ELECTRICAL CHARACTERISTICS - Continued: (T_A=25°C, V_{IN}=12V, C_{DRV}=1.0µF, C_{LDO}=1.0µF, OUTH=OUTL unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{HPW}	*above*		15		ns
t_{LPW}	*above*		15		ns
t_R	C_{OUT}=1nF		10		ns
t_F	C_{OUT}=1nF		3.0		ns
t_{DLH}	*above*		35	50	ns
t_{DHL}	*above*		35	50	ns

DFN3X3 CASE - MECHANICAL OUTLINE





DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.114	0.122	2.90	3.10
B	0.114	0.122	2.90	3.10
C	0.027	0.031	0.70	0.80
D	0.008		0.20	
E	0.0008	0.0011	0.02	0.05
F	0.086	0.106	2.20	2.70
G	0.055	0.07	1.40	1.80
H	0.019		0.50	
I	0.007	0.011	0.18	0.30
J	0.011	0.019	0.30	0.50
K	0.011		0.30	

R0

DFN3X3 (REV: R0)

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LEAD CODE:

Pin Number	Pin Name	Description
1	VIN	Supply Voltage Input. Locally bypass this pin to GND with a ceramic capacitor.
2	LDO	5V LDO Output. This pin provides power to internal logic circuitry and external circuitry up to 20mA. Locally bypass this pin to GND with a ceramic capacitor.
3,6,11	GND	Ground. Internally shorted together.
4	PWM	PWM Input. Receive PWM signal from the controller.
5	PWMB	Inverting PWM Input. Receive inverting PWM signal from the controller.
7	OUTL	Gate Driver Pulldown Output. Connect to the gate of GaN FET and use a resistor to adjust the turn-off speed.
8	OUTH	Gate Driver Pullup Output. Connect to the gate of GaN FET and use a resistor to adjust the turn-on speed.
9	VDRV	Driver Voltage Output. Regulated LDO output from VIN to supply GaN FET gate driver power. Locally bypass this pin to GND with a ceramic capacitor.
10	ADJ	Driver Voltage Adjustment Connect a resistor divider between VDRV and GND to this pin to set the VDRV output voltage.

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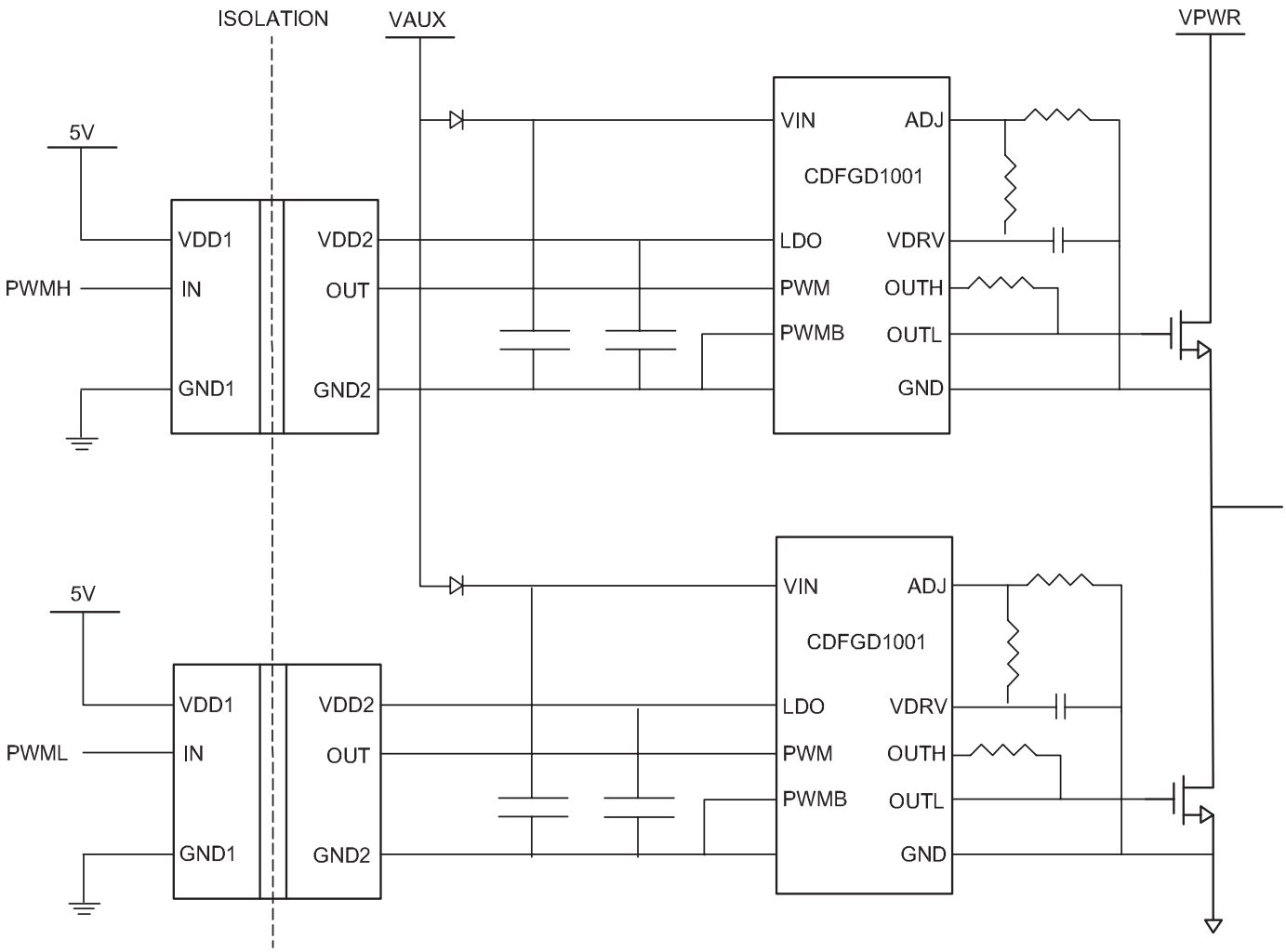
TYPICAL APPLICATION DRAWING



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RECOMMENDED COMPANION CENTRAL GAN FETS

Part Number	Rating	Package	Typical Applications
CDFG6511N	650V, 11.5A	DFN8X8	Lower-current 650 GaN applications
CDFG6517N	650V, 17A	DFN8X8	Mid-power 650V half-bridge / converter designs
CDFG6558N	650V, 29A	DFN8X8	Higher-current 650V GaN applications
CDF56G6511N	650V, 11.5A	DFN5X6A	Space-constrained 650V designs
CDF56G6517N	650V, 17A	DFN5X6A	Compact mid-power 650V designs
CDF56G7032N	700V, 18A	DFN5X6A	Higher-voltage margin applications
CCSPG1560N	150V, 60A	CSP4X6	Low-voltage, high-current GaN designs
CCSPG1510N	150V, 100A	CSP4X6	High-current low-voltage GaN designs

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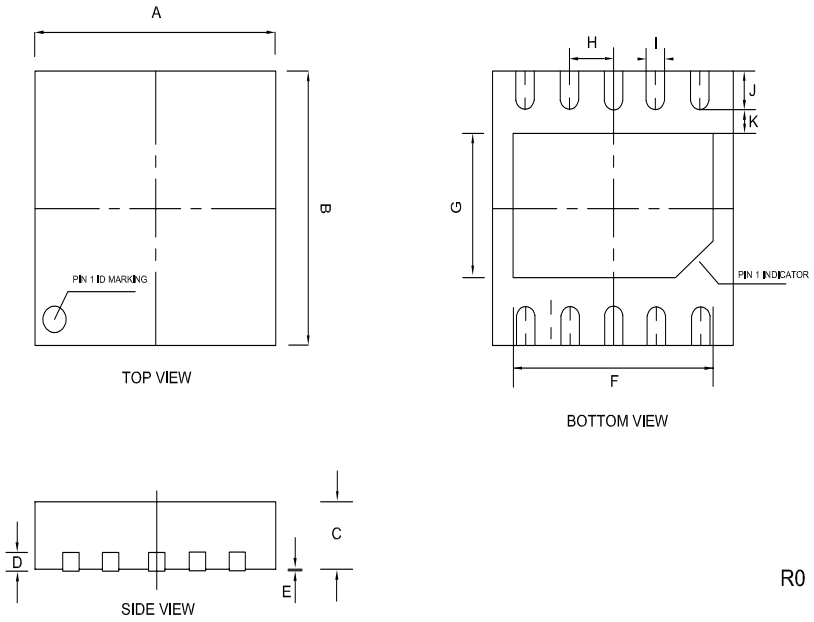
Mechanical Drawing



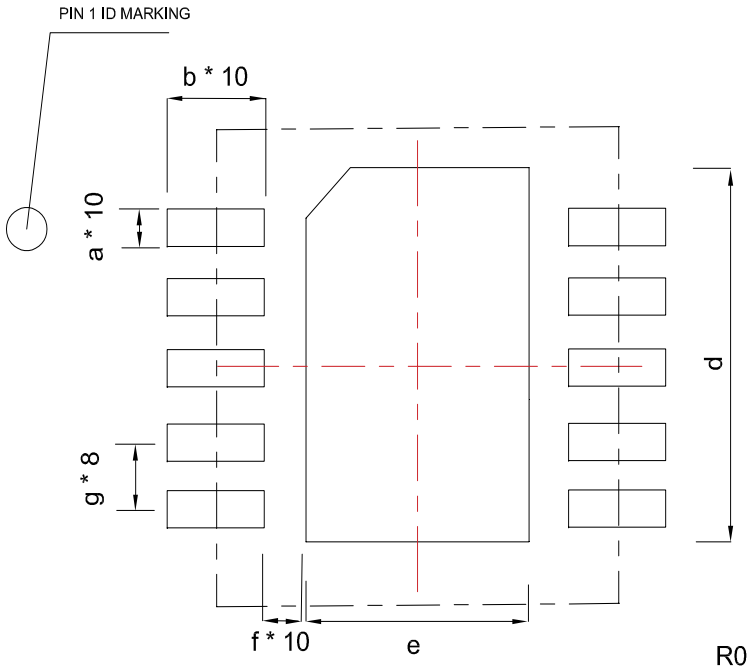
DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.114	0.122	2.90	3.10
B	0.114	0.122	2.90	3.10
C	0.027	0.031	0.70	0.80
D	0.008		0.20	
E	0.0008	0.0011	0.02	0.05
F	0.086	0.106	2.20	2.70
G	0.055	0.07	1.40	1.80
H	0.019		0.50	
I	0.007	0.011	0.18	0.30
J	0.011	0.019	0.30	0.50
K	0.011		0.30	

DFN3X3 (REV: R0)

R0

Part Marking: Line 1: Full Part Number, Line 2: Lot Code, Line 3: Date Code

Mounting Pad Geometry



DIMENSIONS		
SYMBOL	INCHES	MILLIMETERS
a	0.0098	0.25
b	0.0275	0.70
c	0.0098	0.25
d	0.0984	2.50
e	0.0629	1.60
f	0.0118	0.30
g	0.0196	0.50

R0